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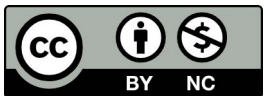

COMMUNICATION

Approaching Gas Phase Electrodeposition: Process and Optimization to Enable the Self-Aligned Growth of 3D Nanobridge-Based Interconnects

*Jun Fang, Leslie Schlag, Se-Chul Park, Thomas Stauden, Jörg Pezoldt, Peter Schaaf, and Heiko O. Jacobs**

The formation of electrical connections between different points in space is a fundamental requirement in any device or system that requires the flow of current. As a consequence and depending on the scale, various free-standing point-to-point electrical wiring methods are used.[1–3] Freeform wires known at the macroscopic scale take on the shape of bondwires at the submilimeter scale, connecting chip-sized objects using wire diameters and contact pads, which can be as small as 10 and 20 µm, respectively.[4] An extension of free-standing point-to-point wiring to a truly microscopic or even nanoscopic scale, however, remains challenging. For example, a nanowire bonding process similar to what will be discussed does not yet exist. Instead, the microelectronics industry uses thin film technologies in combination with lithography to realize the required conductive traces, interconnects or vias between device layers.[5,6] This conventional approach has some disadvantages. First, these are monolithic "on chip" connections which cannot form free-form wire connections between disparate "off chip" parts of a system. Second, and in comparison to wire bonding, an extensive amount of lithographic steps, alignment, and registration are required to form relatively simple electrical connections. Moreover, the majority of the material (including gold, silver, or copper) is wasted during evaporation of the metal and during lift-off or etching. As a consequence and with the aim to reduce material waste, research has been directed toward localized-selected-area-material-deposition concepts often under an umbrella termed as "printable electronics."[7–9] Serial-direct-write deposition techniques belong to this class. Direct write techniques commonly use a (i) liquid[10] or (ii) carrier gas[11] to transport the "electronic ink" to desired locations. Recently, researchers have fabricated free-standing graphene oxide and metallic bondwires to a truly microscopic or even nanoscopic scale.[12,13] However, the process uses an inkjet printing method, which requires individual registration of each bondwire. Consequently, the throughput of serial-direct-write cannot satisfy the manufacturing requirements.

Here, a self-aligned nanowire bonding process[14] to form free-standing point-to-point electrical connections is presented. Wire diameters down to 200 nm and contact pads down to 1 µm will be shown. Moreover, the process is a parallel process to achieve a higher throughput when compared with any of the emerging serial-direct-write or established serial wirebonding methods. The presented process is based on a method that is best referred to as "gas phase electrodeposition." The process has been described in parts before.[15] It is a localized material growth/deposition process which uses charged insulators to attract[17] or deflect[18] an incoming flux of charged material. This is illustrated in **Figure 1** which compares the recently discovered gas phase electrodeposition process with conventional physical vapor deposition. The starting point in both methods is a patterned photoresist or e-beam resist. However, on the right side the material to be deposited (orange particles) is directed to the point of use and no material is lost in subsequent lift-off processes. Some previously reported structures are shown.[15,16]

Taking a closer look at the basic process, it becomes clear that gas phase electrodeposition shares some of the characteristics of electrodeposition in the liquid phase. However, it is a gas phase process with a much larger mean free path of the particles. The Debye length representing the screening length of Coulomb forces is also larger.[19] Despite this difference, it can grow nanostructures in selected domains in a programmable fashion by adjusting the dissipation current of the ionic species that arrive at the surface. For example, it was used to grow straight metallic nanowire arrays whose height and density were adjusted to vary across the substrate which in turn were used as contacts in photovoltaic devices.[16] Others have used this technique to fabricate metallic nanostructures for surface enhanced Raman spectroscopy (SERS).[20,21] In any event, charged material continues to deposit into locations where charge dissipation can occur, leading to a growth of extended structures much like what is observed in the liquid phase based electrodeposition/plating.

This report evaluates the localized growth feature of gas phase electrodeposition as a method to form self-aligned free-standing nanowire interconnects. The optimization of the system is achieved by introducing an improved reactor to adjust the particle size and shape of the emerging structures,

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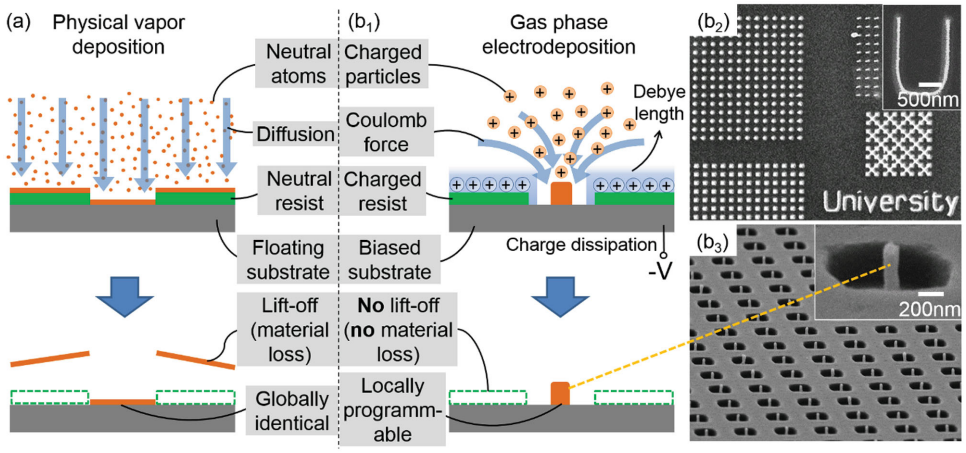

Figure 1. Comparison between a) conventional physical vapor deposition and b) localized gas phase electrodeposition. b_1) Under steady state operation the charged particles deposit locally in the charge dissipating opening. The insulating resist (green layer) has acquired a static surface charge distribution which yields fringing fields whereby the particle are funneled into the charge dissipating openings. No continued buildup of material on the insulating resist was reported as a result: b_2) SEM image where the process was used to prepare a planar (2D) patterned metallic layer containing Au nanoparticles;[15] b_3) SEM image where the process was used to prepare 2.5 D rod-like deposit containing Pt nanoparticles.[16]

as well as electrical conductivity. The relationship between carrier gas flow, primary particle size, and packing density of the growing nanostructured deposits will be discussed and optimized since it led to an increase in the electrical conductivity of the nanostructured deposits when compared to prior results. Moreover, the growing structures can be manipulated by a local electric field to form various 3D geometries. Specifically, the process can be operated in a regime where the Debye length is further increased. As a consequence, it is possible to achieve an enhanced electrodynamic coupling between emanating and growing structures which we tailor to form electrical bridges, leading to the nanoscopic wirebonding idea extending the application ranges. Overall, we find that the gas phase electrodeposition provides an alternative to evaporation with several distinguishing attributes: it supports operation at atmospheric pressure (operation under vacuum is not required), the process is material efficient (material is directed toward the point of use), and the process is locally programmable (instead of globally identical). As demonstrators, we choose the formation of freeform programmable point-to-point nanobridge-based interconnects and the deposition of interdigitated electrode arrays.

Figure 2a describes the programmable gas phase nanomaterial electrodeposition system used in this study. The system is in parts based on the original implementation[15] with the important exception (details discussed later) that it uses a carrier gas flow to transport the charged source material to the substrate and to reduce the particle size beyond previous levels. All the physical dimensions are different as well. The system is enclosed using a N_2 filled acrylic chamber which is kept at atmosphere pressure. The process uses a confined DC arc discharge between two closely spaced electrodes to produce nanoparticles through cathode erosion. The discharge leads to a plasma which surrounds the tip of the consumable cathode. For example, using the depicted 1 mm electrode gap an arc voltage of 1 kV is already sufficient to cause cathode erosion. The sample, typically a 1×1 cm^2 sized silicon or glass substrate with conducting domains is located downstream and collects charged particles.

Figure 2b provides details to explain the current understanding of the process. The sample is typically partially screened using a patterned thin layer of photoresist or e-beam resist (green) with openings to the underlying conducting domains (gray). The openings provide points where material will deposit/grow. The resist (green) prevents charge dissipation and the material seeks to deposit only in the openings. The process can be divided into (i) particle generation, (ii) charging, (iii) global transport, and (iv) localized selected area deposition.

(i) *Particle Generation*: The process of particle formation through cathode erosion using atmospheric pressure arc discharge is well established.[22] Electrons generated in the plasma region are accelerated by the applied electric field to the anode, producing positive gas ions (blue) through impact ionization. The gas ions move and impact the cathode which leads to cathode erosion. We typically increase the voltage until an arc current of 2 mA is established; in nitrogen this will lead to ≈1 kV voltage drop across a 1 mm gap, which is sufficient to achieve cathode erosion in the confined space. For example, after 100 h and Au electrodes we recorded a cathode weight reduction of 3 mg. The resulting average particle diameter is 3 nm (discussed later), which means that approximately 1.4×10^{14} particles are produced per hour to match the weight.

(ii) *Charging*: The eroded material (yellow) leaves the cathode surrounded by a positive space charge region and picks up positive charge resulting in the depicted particle; negative and neutral particles will be present as well (not shown).

(iii) *Global Transport*: in our particular situation, the arc region is modified through the application of a carrier gas jet, which is different from the previously reported design where no carrier gas was used. Previously we used diffusion based transport in combination with Columbic attraction of charged nanoparticles in close proximity to the substrate.

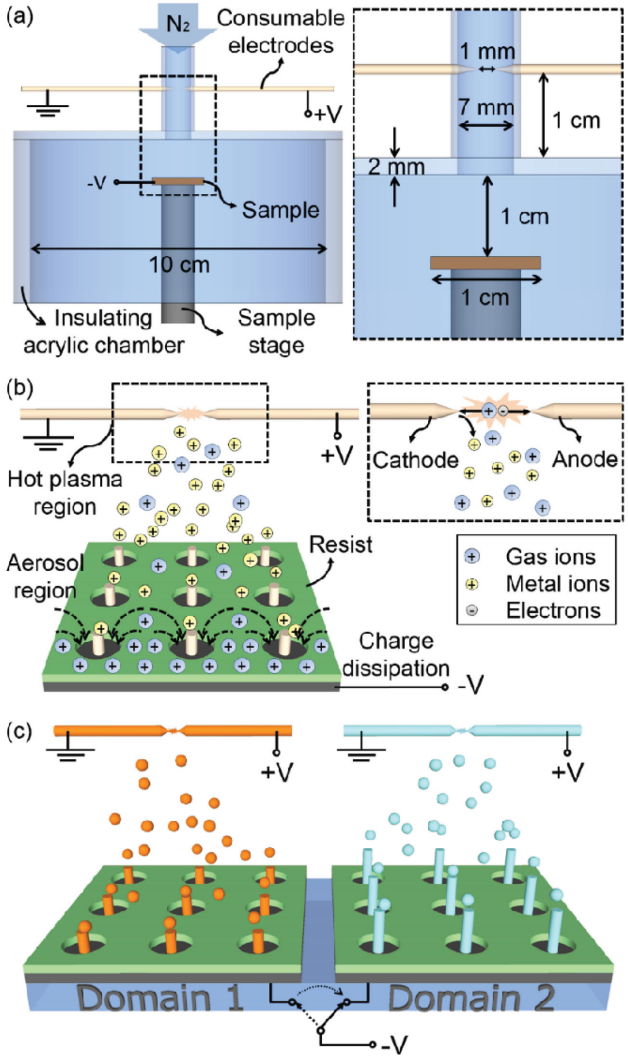

Figure 2. Programmable gas phase nanomaterial electrodeposition system. a) Current setup with dimensions detailing the carrier gas jet, the location of the consumable electrodes, the insulating chamber, and the sample stage. b) Detailed gas phase electrodeposition process: the sample is patterned by an insulating resist (green) with openings to the underlying conducting domains (gray). The openings provide points where material will deposit/grow. The resist prevents charge dissipation and the material seeks to deposit in the openings. c) Programmable electrodeposition concept: domain 1 is turned ON first for a certain deposition time leading to a desired structure (orange); domain 2 is turned ON in a second deposition cycle to receive and grow a different material for an extended period of time leading to a different structure (blue).

The introduced carrier gas appears to play an important role in determining the nanoparticle size and affects the uniformity of the growing structures. Experimentally, we find that the use of a carrier gas leads to the production of smaller particles, which will be discussed later. At the same time it impacts the transport which is now dominated by the flow of the carrier gas transporting the particles toward the substrate.

(iv) *Localized Selected Area Deposition*: This process is possible since all charged species are influenced by nearby electrodes. Depicted is the case for a negatively biased substrate (at a distance of ≈2 cm, $V_{sub} = -1000$ V is commonly used). The deposition process should be considered as an electrodynamic process since the localized field distribution will evolve over time. In the initial stage, an insulating surface will pick up a limited amount of charged material. This in turn will increase the electrical surface potential to reach equilibrium. The resulting electric field will deflect charged particles into the openings. Under steady state, a flux of positive charged material is established which flows to the conducting and bare electrode sites where charge dissipation is possible. Structures will grow only at sites where charge dissipation is possible. The resulting electrical domain current I_d is typically recorded with an electrometer (Keithley, model 6517A).

Moreover, it is possible to use the domain electrodes to collect material at different points in time or for a different duration. This is illustrated in Figure 2c. Domain 1 is turned ON first for a certain deposition time leading to a desired structure length (orange, shown), or film thickness (not shown). Domain 2 is turned ON in a second deposition cycle to receive and grow a different material for an extended period of time leading to a different structure (blue). No shutters are involved. This again is a possibility that does not exist in conventional vapor phase deposition processes where the entire substrate would be coated with a single layer.

The optimization of the system in terms of reducing the average particle size and improving the nanostructure is studied. Different from prior implementations,[16] we used a carrier gas (N_2) in the current reactor. Experimentally, we find that the use of a carrier gas leads to the production of smaller particles and growing structures that have an increased density and improved electrical conductivity.

Figure 3 identifies the carrier gas flow as one of the key parameters in the optimization of gas phase electrodeposition since it affects the smoothness of the growing structures. Specifically, we discovered a clear dependence between carrier gas flow and (a) shape of the growing structures, (b) dissipation current at $V_{sub} = -1000$ V, and (c) particle size distribution. As mentioned before, the particles originate in the discharge region that is confined using a 7 mm inner diameter tube. The N_2 carrier gas was purchased from Matheson (UHP/ZERO GRADE, 99.999%). The gas flow rate was controlled by a digital gas flow meter. The temperature and the humidity in the experiment were set approximately to be 22 °C and 50%, respectively. All metals we have tested show two operating regimes leading to either dendritic high surface-to-volume ratio structures or dense metallic deposits:

(i) "Low-carrier-gas-flow regime" represents the condition where a clear increase in the primary particle size (sometimes exceeding 10 nm) is observed and where the size distribution is larger. This in turn leads to a dendritic growth (a, left side). This statement is correct for all metals we have tested (shown: Au, Ag, Cu, not shown: Rh, In, Pt, Co, Mo, Re, Ru, Zn). These structures have a high surface-to-volume ratio and should be useful for any catalytic process, like batteries or cells for water splitting applications.[23] An

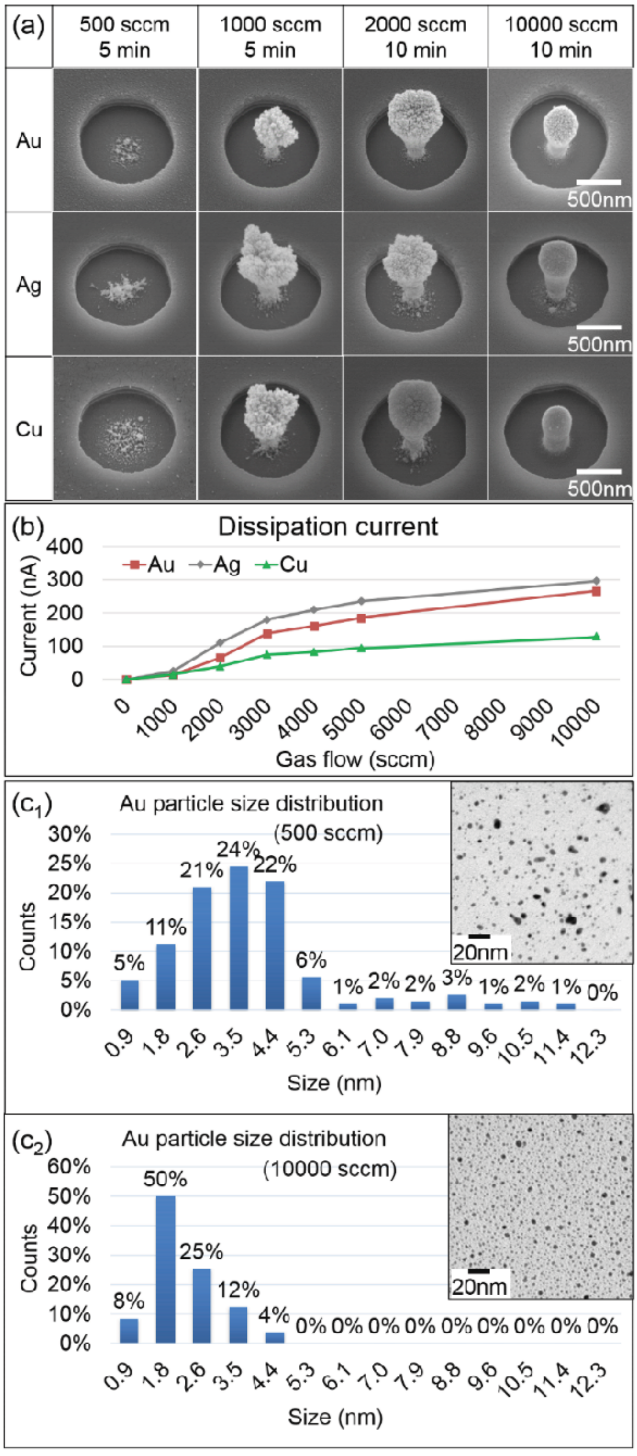

Figure 3. Shape of the emerging structure, ionic substrate current, and primary particle size distribution as a function of carrier gas flow. a) SEM images depicting Au, Ag, and Cu deposits; the uniformity of the emerging structures improves with an increase in the carrier gas flow. b) Graph of the dissipation current as a function of gas flow: a higher flow rate results in a larger dissipation current. c) Histograms and TEM images depicting the Au particle size distribution at c_1) 500 sccm with 3.9 nm average diameter and 2.4 nm STD and c_2) 10 000 sccm with 2.2 nm average diameter and 0.8 nm STD.

exemplary histogram of the size distribution selecting the Au nanoparticles is shown in (c_1). An average diameter (3.9 nm) and standard deviation (2.4 nm) was recorded in this case (experimental conditions were 500 sccm N_2, 2 mA arc current, 1 kV arc voltage, 8 nA dissipation current, and 10 min collection time, TEM analysis counting 100 particles collected on a TEM grit).

(ii) "High-carrier-gas-flow regime" represents the condition where a clear reduction in the primary particle size (typically smaller than 5 nm) is observed and where the standard deviation is reduced. This in turn leads to deposits and growing structures that are dense (a, right side). Again all metals we have tested showed this behavior. These structures provide an increased mechanical stability and electrical conductivity (discussed later). An exemplary histogram of the size distribution selecting the Au nanoparticles is shown in (c_2). Both the average diameter and standard deviation reduced from 3.9 to 2.2 and 2.4 to 0.8 nm, respectively (experimental conditions were 10 000 sccm N_2, 2 mA arc current, 1 kV arc voltage, 260 nA dissipation current, and 10 min collection time, TEM analysis counting 100 particles collected on a TEM grit).

The discovered "carrier gas – particle size – structural and electrical property relationship" can be explained: With an increased carrier gas rate, an increased cooling rate around the arc region will be present, which should lead to smaller particles. Moreover, the arc shows more fluctuation leading to a visible movement of the "anchor" points at the electrodes at higher flow rates. As a consequence, the point of erosion will fluctuate and this should lead to shorter localized heating/erosion before the anchor point jumps to a new erosion point. In addition, the primary particles reach the sample surface faster, which should lead to a reduction in "arc & in-flight aggregation." This explains the observed results: arrival of isolated round particles (c_2, TEM inset) at high flow rates and a higher packing density.

The previously mentioned reduction of arc & in-flight aggregation is believed to be the primary factor to explain the increased packing density of growing structures in the high-carrier-gas-flow regime. This argument is also supported by the TEM images (c, insets). At low-carrier-gas-flows and short exposure times (<1 min) we find isolated relatively large aggregates on the TEM grit. The size of these aggregates appears to be independent of the collection time. In other words, they must form in the arc region or in-flight before they arrive at the surface. For example, we tested 10, 20, and 40 s and found >10 nm sized aggregates in each case which contained small (<3 nm) primary particles in the low-carrier-gas-flow regime. Growing structures, which are building up through continued collection of these large aggregated particles, are fluffy because of geometric hindrance. Furthermore, the recorded dissipation current is low despite the fact that the structures grow relatively quickly, which means that the charge/particle size ratio is much smaller in the low-carrier-gas-flow regime when compared to the high-carrier-gas-flow regime.

We believe that the suppression of arc & in-flight aggregation is the dominating factor in increasing the packing density in

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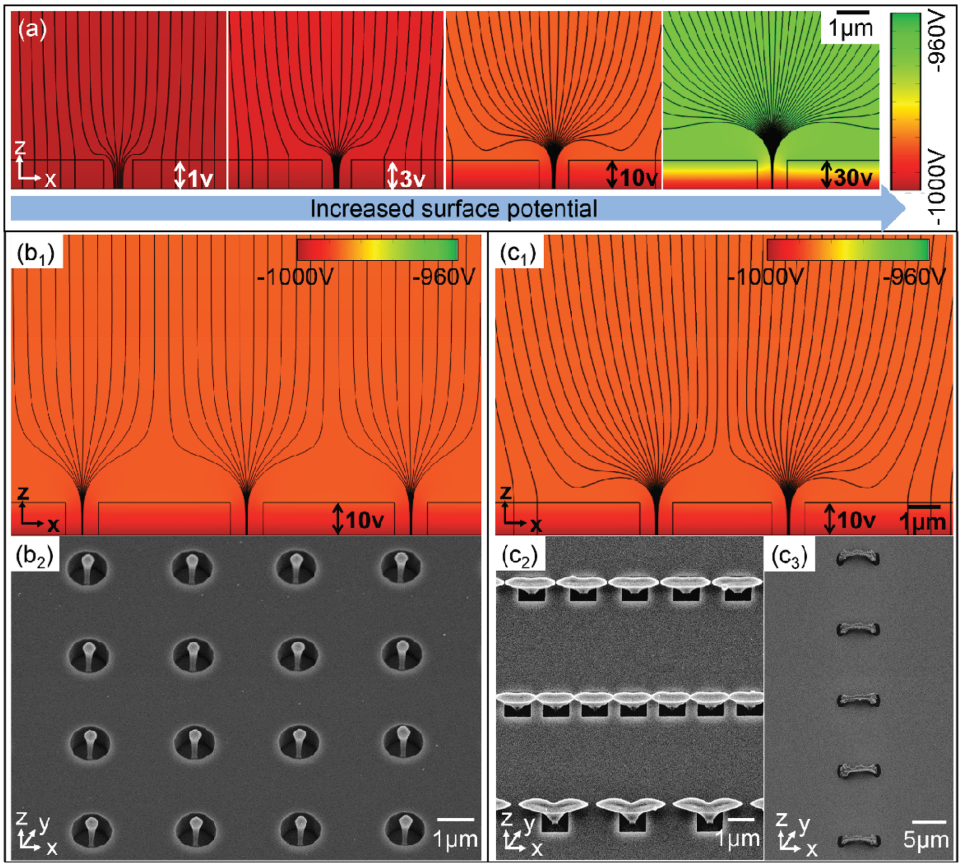


Figure 4. Nearest neighbor interaction: a) Computed electric field distribution at different resist surface potentials and localized gas phase electrodeposited copper structures comparing b) equally spaced (5 μm pitch) and c) unequally spaced openings inside a 1 μm thick photoresist. An increase in the surface potential leads to an increased focus of the electric field lines. Unequal distances between nearest neighbors lead to the formation of copper bridges in the experiments. c_2) The upper and lower rows show an intermediate state where the bridge is not completely closed; 30 nm gaps (upper row) and 200 nm gaps (lower row) are visible; the gap distances are uniform from one location to the next. c_3) Wires bridging an 8 μm gap.

the high-carrier-gas-flow regime. However, another explanation exists which cannot be excluded. The second explanation considers the electrical mobility of charged particles. The current arrangement with a nozzle pointing down to the parallel plate is known to acts as a filter[24] that can attract particles based on the size or more specifically differential mobility. The arrangement favors charged particles with small diameter, which have a high electrical mobility and are preferentially attracted toward the surface. However, we do not believe that the effect of differential mobility plays an essential role in our case, otherwise we should see particle size gradient away from the center of the substrate collecting larger particles toward the edge. This is not observed. Moreover, we should see a reduction of the ionic current at higher flow rates since fewer particles will reach the surface. The opposite is the case. As a consequence and for the reasons mentioned before, the suppression of arc & in-flight aggregation in the high-carrier-gas-flow regime is believed to be the primary reason why the packing density, structural stability, and electrical conductivity improve. In other words, the arrival of isolated and smaller particles is the primary reason.

To sum up, the optimization of the gas phase electrodeposition system is realized by introducing a carrier gas (N_2) in the current reactor, along with a redesigned reaction chamber. Both experimental results and theoretical analysis show that the generated particle size is reduced and the shape of the emerging structure is improved. This optimization provides a possibility to form point-to-point nanobridge-based interconnects and interdigitated electrode arrays that will be discussed later.

Another interesting discovery deals with the screening length and nearest neighbor interaction. In the wet chemical electrodeposition, which shares some similarities, the Debye length is often used as measure to determine the screening length. It is commonly smaller than 10 nm and nearest neighbor interaction is limited. This is different in the discovered gas phase electrodeposition process. Nearest neighbor interaction can take place at much larger distances (10 μm in some cases). This supports a different set of applications. **Figure 4** provides some understanding on the effect of nearest neighbor interaction comparing computed electric field distributions with deposition results using a 1 μm thick photoresist (MICROPOSIT S1800) with 1 μm sized openings to a Si substrate. The Supporting Information provides more details on the computation. The calculated field is shown for five different constant values (1, 3, 10, 30 V) of the surface potential; the actual level of the surface

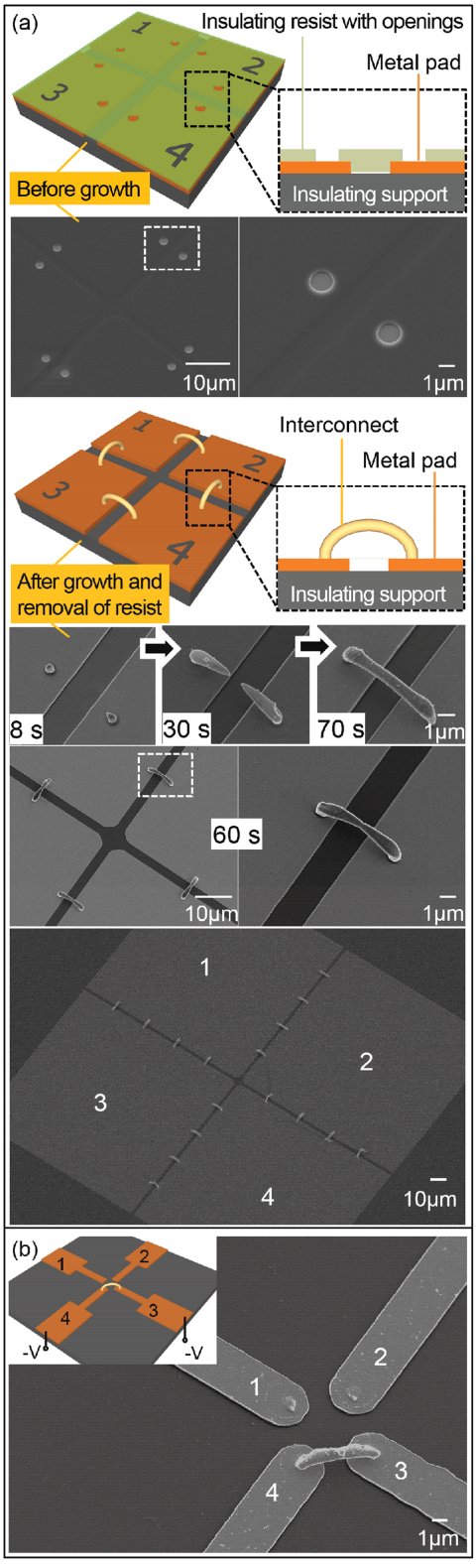


Figure 5. Programmable growth of self-aligned free-standing nanobridge-based interconnects: schematics and corresponding results before and after growth. a) Nanobridge-based interconnects applied to electrically connect four different 100 μm × 100 μm squared metal pads. A 200 nm thick insulating PMMA resist (green layer) defines several 1 μm in diameter contact points with a 5 μm gap. SEM images after Au growth and removal of the resist showing the structures after 8, 30, 70, and 60 s long deposition. Overview SEM images showing a total of 16 (4 × 4) Au interconnects. b) Nanobridge-based interconnect grown in a programmable fashion. Metal pads 1 and 2 are left floating which prevents charge dissipation and continued growth (growth is turned OFF). Inset: Schematic of experiment and bias voltages, terminal 3 and 4 are biased negatively, growth is turned ON and electrodes 3 and 4 are connected with a 5 μm long Au nanowire.

potential and distribution along the surface is unfortunately not known. From a computation point of view, an increase in the surface potential (Figure 4a, compare far right with far left image) leads to: (i) an increased focus of the electric field lines and (ii) fewer field lines which impinge on the insulating resist surface. The depicted impinging field lines are present at the outset of the experiment (Figure 4a, left). However, this will lead to a pick-up of positive charge, which in turn increases the surface potential and leads to a field distribution with fewer impinging field lines (Figure 4a, transitioning from left to right). In other words, in the experiments the insulating resist picks up positive ions and particles to a point where the surface potential has increased to a sufficiently large value to divert the flux of positive particles to the charge dissipating openings. A 1 μm thick layer of photoresist (MICROPOSIT S1800) has a breakdown strength of ≈400 V μm^{-1}[25] and can thus float up to a sufficiently high value to divert the flux of charged particles.

This general behavior is visible in all experiments where the insulting resist is intact and not leaking. The shape of the growing structures (Figure 4b,c) agrees well with computed field distribution (experimental conditions were: 2 mA arc current, 1 mm gaped copper electrodes, 10 000 sccm of N_2, 130 nA ionic substrate current, and 10 min long deposition). Openings which are evenly spaced in the x and y direction (b) lead to a field distribution and growth pattern which points primarily in the z direction. Coupling to the nearest neighbors becomes visible as the growing structure leaves the photoresist guides, which can be used to grow asymmetric structures.

From a material deposition point of view, the observed growth behavior can be explained. It agrees with a material transport which arrives globally from the top in all cases. However, in Figure 4c the flux is divided into 2D sheets, which are in line with the rows of openings, before the sheets are broken down into individual filaments. This type of transport leads to the observed forking (c_2) and ultimately to the formation of interconnects between nearest neighbors (c_3).

The growth rate depends on various parameters. One of them is the density of the openings, which was approximately the same in (b_2 and c_2). The structures are about 2 μm long from the beginning to the end, which represents a growth rate of 200 nm min^{-1}. The number of openings per area was smaller in (c_3) leading to a slightly larger rate of approximately 400 nm min^{-1}. A different condition where the growth rate is >10 times higher will be discussed in the next paragraph.

Figure 5 shows the schematics and corresponding results where the general strategy of gas-phase nanoparticle electrodeposition is applied to grow self-aligned free-standing nanobridge-based interconnects. A Si substrate with a 100 nm thick Si_3N_4 layer is used in this experiment. The insulating Si_3N_4

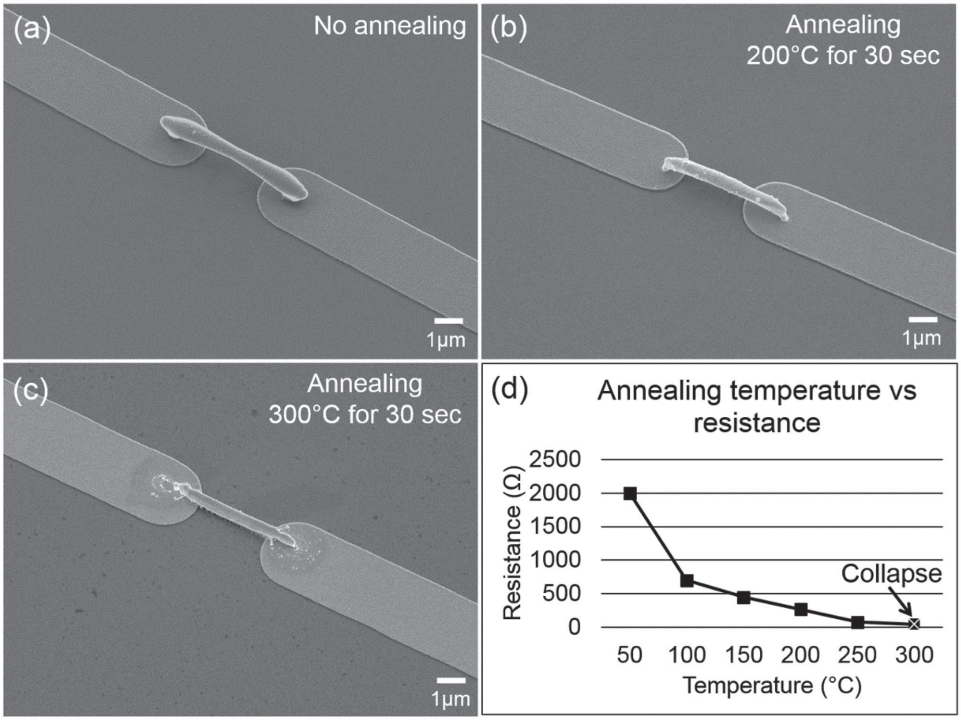


Figure 6. SEM images and total resistance of Au nanobridge-based interconnects with and without annealing. SEM images a) before and after a 30 s long annealing step at b) 200 °C, and c) 300 °C in nitrogen; the bridges begin to break at 300 °C due to shrinkage. d) A plot of resistances at different annealing temperatures.

layer supports four contact pads. We use conventional e-beam evaporation Cr/Au (20/50 nm) and photolithography to prepare these relatively large pads. The structure shows pairs of 1 μm in diameter contact points with one contact on each pad. The contact points are openings in an insulating 200 nm thick PMMA layer which we defined using e-beam lithographically. The goal was to grow freeform self-aligned nanowire bridges in between these locations. Results represent 2 mA arc current, 1 mm gaped Au electrodes, 10 000 sccm of N_2, and 260 nA ionic substrate current. Interestingly, a 1 min long deposition time was sufficient to grow the bridge across the 5 μm long gap. In other words, the growth rate was 2.5 μm min^{-1}. This is a factor of ≈12.5 higher when compared with the experimental results presented in Figure 4b_2,c_2. The primary reason for the higher rate is the lower number of openings per area in the insulating resist where charge dissipation takes place. Generally speaking, the smaller the area and number of electrical contact points, the larger the growth rate. This is because the particle generation rate is constant. The observed behavior can be explained if all or most of the generated particles are collected. A smaller number of collection points lead to a higher localized material flux rate, resulting in a higher localized growth rate of the wires.

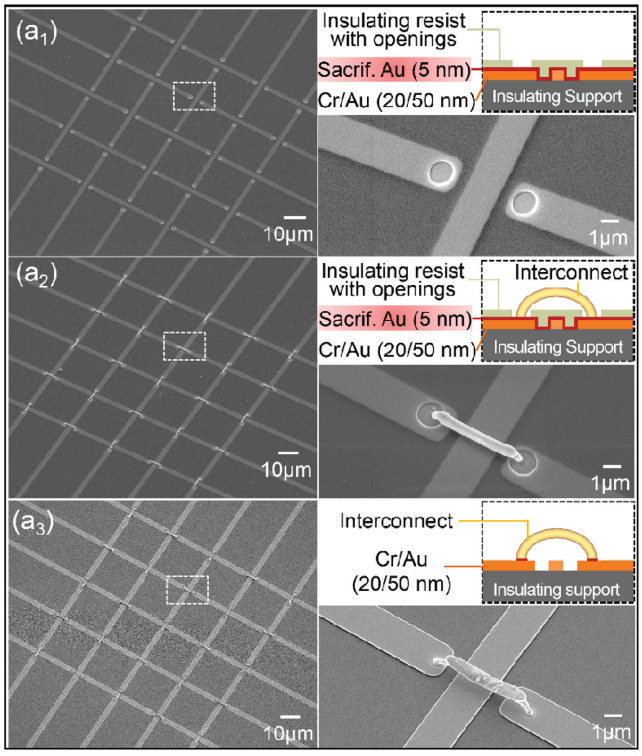
The grown structures and bridges were found to be fairly robust. We were able to remove the PMMA layer in acetone, washing the chips in IPA, and drying them under a stream of dry nitrogen without losing them. In Figure 5a, all bridges were grown at the same time. The goal was to test the uniformity and the bridges looked alike in the SEM across the 200 μm × 200 μm area. In Figure 5b, the idea of programmable growth is tested. The goal was to evaluate if it is possible to grow a free-standing nanobridge-based interconnect at a predetermined location. To achieve this goal we applied a negative bias to terminal 3 and 4; at the same time we left terminal 1 and 2 floating. The deposition condition is identical to the previous experiment (2 mA arc current, 1 mm gaped Au electrodes, 10 000 sccm of N_2, and 260 nA ionic substrate current, 1 min). Floating terminals block charge dissipation and growth at this location. Careful analysis, however, shows small amounts of unexpected precipitation on the floating pads 1 and 2. So some charge dissipation must have taken place. A possible dissipation path could involve leakage through the 100 nm thin nitride layer.

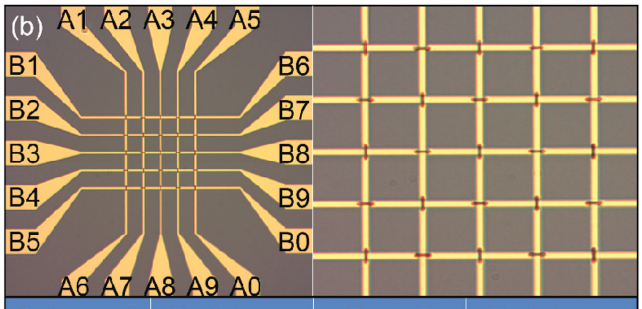
Figure 6 shows SEM images of interconnects (a–c) next to a graph (d) of the measured resistance before and after annealing. The annealing is done in a rapid thermal annealer (RTP-600S, heated by tungsten-halogen lamps) under nitrogen. Results represent a nanobridge-based interconnect spanning a 5 μm gap grown in 1 min using the same conditions as described in Figure 5. Without annealing (a) the bridges had a fairly large resistance with values of a few kΩ, which is larger than what we hoped. However, a fairly small annealing temperature on the order of 200 °C (b) is sufficient to reduce the resistance by a factor of 10 achieving less than 200 Ω. An annealing temperature of 250 °C has been determined as safe to maintain the integrity of the depicted interconnects leading to a resistance of approximately 85 Ω or a factor of 23 when compared with the unannealed structures. These are the smallest values both in terms of required annealing temperature and achieved resistance we have achieved so far. The single most important parameter has been the reduction of the

primary particle size. Prior structures which contained larger particle had a lower packing density and had poor electrical and mechanical properties.[16]

However, there is still room for improvement. The theoretical limit is 0.56 Ω (calculated using $R = \rho l/A$ with l = 5 µm, cross-section $A = \pi(0.25\ \mu m)^2$, and $\rho_{Au} = 2.2 \times 10^{-8}\ \Omega$ m). We believe that a further reduction of the primary particle size is required to approach this limit. At present the particles have a diameter ranging from 1 to 5 nm. While the density has improved the growing structures are composed of nanoparticles and some level of porosity is likely remaining. In other words the structures have a higher level of porosity when compared to vapor deposition of single atoms. The assumption that some level of porosity is still remaining is consistent with the fact that a small amount of shrinkage is visible in the SEM images after heat treatment. For example at 300 °C the shrinkage can lead to mechanical stress and subsequent failure of the attachment points and even collapse of the structures (c).

Figure 7 shows images of a 5 × 5 interdigitated electrode array test structure which requires the growth of 25 isolated crossovers between the rows and columns. The rows and columns are on the same layer. Two ideas are being tested. The first idea is to evaluate if crossovers can be fabricated with fewer processes and alignment steps than commonly necessary. Conventional realization of crossovers requires: (i) deposition; registration and patterning of an insulator; (ii) via plating and polishing; and (iii) deposition, registration, and patterning of a top conductive layer. In comparison, our approach replaces steps (ii and iii) with a single registration-free gas-phase-electrodeposition step. The second idea behind the design is to test if daisy chains of bridges lead to a total resistance which is a multiple of the resistance of an individual interconnecting bridge as previously recorded in Figure 6. Consequently, the same processing conditions were used in this experiment with one exception. Specifically, the test structure contains several strips of metallic conductors (electrically isolated sections of rows and columns). No electrical bias can be applied to these regions and charge dissipation and growth will not occur. As a result the concept of gas phase electrodeposition is not possible in these areas. However, a solution from the wet chemical counterpart can be borrowed. Like in wet chemical electroplating a thin sacrificial charge dissipating metallic layer (red layer in the insets) underneath the resist (green layer) is required to plate metal at the locations where the vias are present. We used a 5 nm thin layer of evaporated Au to support temporary charge dissipation and crossover nanowire growth (a_1). Like in previous experiments, the nanowires are grown within 1 min with the same deposition condition (a_2). Subsequently, the PMMA layer is removed in acetone and the substrate is immersed in GE-6 gold etchant for 10 s to remove the thin gold sacrificial layer. The nanowire remain intact due to a short etch time. The samples are annealed at 250 °C for 30 s leading to the final structure (a_3). Figure 7b shows an overview optical microscopy image with overlaid pad labels and a table with measured values of the total resistance. The measured total resistance depends on the number of crossovers in each daisy chain. Depending on the location of the row or column there are either two or three crossovers in this array. Out of the 25 crossovers all were electrically intact. On average, each crossover accounts to about 85 Ω.





Columns A	Resistance	Rows B	Resistance
A1-A6	283 Ω	B1-B6	181 Ω
A2-A7	162 Ω	B2-B7	255 Ω
A3-A8	267 Ω	B3-B8	177 Ω
A4-A9	155 Ω	B4-B9	248 Ω
A5-A0	239 Ω	B5-B0	150 Ω
$A_i - B_j = \infty$			

Figure 7. Gas phase electrodeposition applied to grow self-aligned interdigitated electrode arrays: SEM images, optical images, and resistance values. SEM images show the test structure with 25, crossovers a_1) before growth, a_2) after growth, and a_3) after removal of the resist and Au sacrificial layer. Each bridge growth across the intersecting electrode without touching it. b) The table lists the total resistance measured between the terminals depicted in the overview optical microscope image; on average a bridge contributes 85 Ω to the total resistance which is either 170 Ω or 250 Ω depending on the number of crossovers in the daisy chain. $A_i - B_j = \infty$ means that no leakage current was detected between the columns and the rows.

Moreover, no electrical shorts between the columns and rows were detected indicating that the crossovers are not in contact with the electrodes underneath.

A novel nanowire bonding processes to grow free-standing point-to-point electrical connections has been demonstrated. The process is based on a gas phase electrodeposition concept, which is a localized material growth/deposition process where a patterned insulating resist is used to control charge dissipation. The process is more material efficient when compared to conventional vapor deposition since the material is directed to the point of use. No lift off is required.

The nanoparticles were produced using an arc discharge based plasma. Here the use of a carrier gas was discovered as an important parameter to reduce the primary particle size below a 3 nm threshold. Moreover, the carrier gas reduced in-flight-aggregation which in turn improved the density, mechanical, and electrical property of the growing nanostructures. Electrical measurements are now possible due to the improved mechanical and electrical characteristics.

The resistivity in the case of Au deposits is presently about 7.9×10^{-5} Ω m without annealing and 3.3×10^{-6} Ω m with annealing at 250 °C (calculated using the measured resistance and dimensions $l = 5$ µm and $r = 250$ nm). While it is the first time electrical measurements have been reported the values are still by a factor of 150 higher than the bulk resistive 2.2×10^{-8} Ω m of gold indicating that there is room for improvement. We believe that a reduction of the primary particle size into the sub 1 nm range is likely going to continue to improve the electrical and mechanical properties. However, the exact methodology how to achieve the required reduction in the primary particle size is not yet known. Possible solutions could be an increase in the gas flow beyond the levels reported in this publication, the use of a different or cooled carrier gas, changes in the localized flow velocity surrounding the arc region, a reduction of the arc power, and changes in the pressure. The study and optimization of this parameter space requires the design of an improved gas phase electrodepositing system. Alternatively, a further improvement of the conductivity and mechanical properties could be achieved through an in situ annealing approach; for example, through the incorporation of a flash lamp annealing methodology, or a temperature controlled and heated substrate or deposition chamber.

The discovered nearest neighbor coupling effect supports the growth of bridges. The growth of bridges is possible due to an increased screening length when compared to the wet chemical counterpart where a high ion concentration screens charges within a few nm. Nearest neighbor coupling across a 10 mm gap has been possible. This finds applications. The demonstrated freeform programmable point-to-point nanobridge-based interconnects, and the deposition of interdigitated electrode arrays are two examples. In the future it should be possible to extend this further, it should be possible to create 3D free-standing nanowire structures and freeform wire connection between disparate "off chip" parts of a system. The formation of vias between device layer through gas-phase deposition should also be possible.

While the applications are apparent we feel that the understanding of the deposition process remains fairly limited. The effect of pressure, carrier gas temperature, substrate temperature, gas ion concentration, insulting resist type and thickness, and humidity on the growth process, for example, is not known. The ultimate level of precision or conductivity that can be reached is also not known.

Experimental Section

Chamber and Arc Discharge: The current setup (Figure 2) used a carrier gas jet with gas flow rates between 20 and 20 000 sccm nitrogen. The gas inlet had 7 mm inner diameter. The consumable electrodes were located in the carrier gas jet inlet 10 mm in distance to the insulating chamber. The inner diameter of this chamber was 100 mm. The walls were at least 2 mm thick. The sample stage was located 10 mm underneath the gas inlet, 20 mm in distance from the consumable electrodes. The applied electrical current between anode and cathode was 2 mA, in nitrogen this lead to 1 kV voltage drop across a 1 mm gap. After 100 h and Au electrodes the cathode weight reduction was 3 mg. Various types of metals were used, we tested Au, Ag, Cu, Rh, In, Pt, Co, Mo, Re, Ru, and Zn. The metals were ordered as wires with 1 mm diameter at Advent Research Materials, except Ru, which is available from Goodfellow as 2 × 2 mm thick bars. The corresponding dissipation currents at specific gas flow rates are shown for Au, Ag, and Cu in Figure 3. The resulting electrical dissipation current, I_d was recorded with a Keithley, model 6517A.

Particle Size Distribution: The particles were collected on Quantifoil S7/2 copper 300 mesh substrates. These foils were analyzed by a TEM TECNAI model S20 with Gatan filter. Particles were man-counted and man-measured in an area of 500 × 500 nm at different sites of these foils. The resulting average particle diameter was 3 nm, which means that approximately 1.4×10^{14} particles were produced per hour to match the weight.

Substrate Preparation: To grow metallic nanowire directly on Si wafer, the Si wafer (P-type, 0-100 Ω cm) was cleaned by acetone, IPA and DI water. The wafer was then patterned by photoresist (MICROPOSIT S1800). The thickness of the photoresist depends on the spin speed during the coating process. To form nanobridge-based interconnects on the substrate, a Si_3N_4 insulating layer (1000 Å) was first grown on Si wafer. Conventional e-beam evaporation and photolithography was used to prepare Cr/Au (20/50 nm) layer. E-beam lithography was then used to pattern PMMA insulating layer with openings at desired location.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] G. Harman, J. Albers, *IEEE Trans. Parts, Hybrids, Packag.* **1977**, *13*, 406.
[2] K. Toyozawa, K. Fujita, S. Minamide, T. Maeda, *IEEE Trans. Compon., Hybrids, Manuf. Technol.* **1990**, *13*, 667.
[3] A. C. Fischer, J. G. Korvink, N. Roxhed, G. Stemme, U. Wallrabe, F. Niklaus, *J. Micromech. Microeng.* **2013**, *23*, 083001.
[4] C. E. Tan, J. Y. Liong, J. Dimatira, L. W. Kok, J. Tan, L. H. Wijaya, K. H. Kwong, *Electron. Packag. Technol. Conf.* **2014**, *16*, 107.
[5] T. N. Theis, *IBM J. Res. Dev.* **2000**, *44*, 379.

[6] S. J. Ok, C. Kim, D. F. Baldwin, *IEEE Trans. Adv. Packag.* **2003**, *26*, 302.
[7] B.-J. de Gans, P. C. Duineveld, U. S. Schubert, *Adv. Mater.* **2004**, *16*, 203.
[8] Z. Fan, J. C. Ho, T. Takahashi, R. Yerushalmi, K. Takei, A. C. Ford, Y.-L. Chueh, A. Javey, *Adv. Mater.* **2009**, *21*, 3730.
[9] J. Mei, M. R. Lovell, M. H. Mickle, *IEEE Trans. Electron. Packag. Manuf.* **2005**, *28*, 265.
[10] J. Bharathan, Y. Yang, *Appl. Phys. Lett.* **1998**, *72*, 2660.
[11] L. Wang, J. Liu, *ECS J. Solid State Sci. Technol.* **2015**, *4*, 3057.
[12] J. H. Kim, W. S. Chang, D. Kim, J. R. Yang, J. T. Han, G.-W. Lee, J. T. Kim, S. K. Seol, *Adv. Mater.* **2015**, *27*, 157.
[13] B. W. An, K. Kim, H. Lee, S.-Y. Kim, Y. Shim, D.-Y. Lee, J. Y. Song, J.-U. Park, *Adv. Mater.* **2015**, *27*, 4322.
[14] J. Ji, Z. Zhou, X. Yang, W. Zhang, S. Sang, P. Li, *Small* **2013**, *9*, 3014.
[15] J. J. Cole, E. C. Lin, C. R. Barry, H. O. Jacobs, *Small* **2010**, *6*, 1117.
[16] E. C. Lin, J. J. Cole, H. O. Jacobs, *Nano Lett.* **2010**, *10*, 4494.
[17] H. O. Jacobs, G. M. Whitesides, *Science* **2001**, *291*, 1763.
[18] A. M. Welle, H. O. Jacobs, *Appl. Phys. Lett.* **2005**, *87*, 263119/1.
[19] C. R. Barry, H. O. Jacobs, *Nano Lett.* **2006**, *6*, 2790.
[20] E. C. Lin , J. Fang , S. C. Park, T. Stauden , J. Pezoldt, H. O. Jacobs, *Adv. Mater.* **2013**, *25*, 3554.
[21] J. Fang, S. C. Park, L. Schlag, T. Stauden, J. Pezoldt, H. O. Jacobs, *Adv. Funct. Mater.* **2014**, *24*, 3706.
[22] B. M. Smirnov, *Physics of Ionized Gases*, Wiley, New York, **2001**.
[23] S. W. Boettcher, J. M. Spurgeon, M. C. Putnam, E. L. Warren, D. B. Turner-Evans, M. D. Kelzenberg, N. S. Lewis, *Science* **2010**, *327*, 5962.
[24] G. A. Sehmel, U.S. 3879986 A **1975**.
[25] S. Biswas, *Master Thesis*, Lund University, **2013**.